

CVC Verilog Simulator delivers high performance and capacity to the most demanding IC designers. Adhering to industry standard IEEE Verilog, CVC compiles into native machine code providing maximum simulation performance. Its ease-of-use, plus the ability to simulate in interpreted or compiled modes makes it an important addition to your design flow.

## Optimizing Compiler

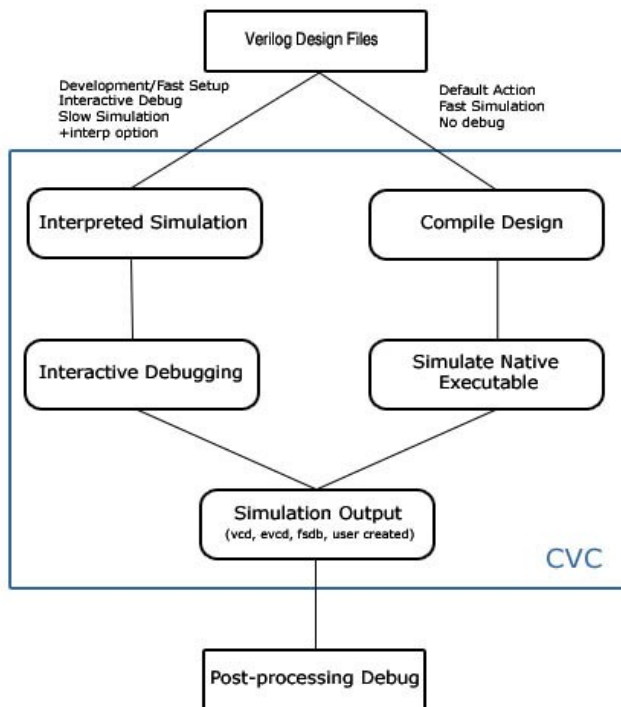
CVC's optimizing compiler technology provides fast native code performance and large design capacity. CVC uses efficient flow graph based algorithms to quickly compile even the largest designs into machine code executables. In one simple step, CVC compiles using optimizations at the RTL and gate-level to create a fast simulating executable. Using optimizations to take advantage of modern hardware, CVC's simulation speed rivals any available compiled simulator without sacrificing simulation result accuracy. CVC's simple compilation eliminates the complex linking and loading steps performed by other Verilog simulators.

## CVC Advantages

- ◆ IEEE 1364-2005 compliant simulator
- ◆ Fast native compiled simulation
- ◆ Interpreted or compiled simulation
- ◆ Large gate capacity
- ◆ Full PLI (vpi\_, acc\_, tf\_) support
- ◆ Flexible licensing

## Compiled or Interpreted Simulation

In addition to CVC's native code compiler technology that allows more exhaustive design testing, CVC provides the ability to run in interpreted mode resulting in very fast design elaboration. Before long regression simulations can be run, it may be necessary to debug or verify Verilog models. Simulating in interpreted mode eliminates compile time during early design stages when Verilog source code is frequently modified. Eliminating compilation gives CVC the ability to load the largest designs in only a few seconds. Additionally, interpreted mode allows interactive Verilog statement level debugging.



When simulation speed is critical, CVC compiles a design into a native executable in one simple step. The resulting executable can then be used to run multiple simulations. Compilation is only required when a design changes. CVC eliminates the need to build complex libraries prior to design compilation. Compiled simulation is fast and speed competitive with the fastest compiled simulators on the market. Performance and price make CVC ideal for large regression server farms when throughput per license is of the utmost importance.

## SPECIFICATIONS

### SIMULATION

- Native compiled to machine code architecture
- Full IEEE P1364-2005 Verilog standard support
- Interpreted mode
- Creates compiled executable allowing multiple simulation runs without recompilation
- High capacity and efficient CPU memory and cache usage
- 64-bit mode allows large gate-level designs

### INTERFACES

- Comprehensive and efficient PLI support
- Full SDF support

- FSDB format

### PLATFORMS

- Linux
- Mac OS X
- 32/64-bit

### LICENSING

- Flexible licensing options
- 32/64-bit maximum capacity/performance for one low price
- Notebook licensing

### Flexible Debugging Features

- VCD/EVCD/FSDB value change dump formats

- Supports Verilog-XL™ style command debugger with GDB programming language extensions in interpreted mode
- Supports both statement and edge break points with conditional expression and instance selection filters

### FURTHER INFORMATION

For further information on CVC please visit us on the web.

[www.pragmatic-c.com](http://www.pragmatic-c.com)