

Pragmatic C Software Announces Fast P1364 Verilog Compiler

MINNEAPOLIS, April 13 /PRNewswire/ -- Pragmatic C Software Corporation announced today the immediate availability of its new high performance Verilog HDL P1364-2005 simulator called CVC.

Dual Mode Compiled and Interpreted Simulation

CVC combines the simulation speed of modern compiled Verilog simulators with the convenience of legacy Verilog XL style simulators. Compiled CVC translates Verilog HDL designs into native machine code which is then executed for exhaustive design verification. In interpreted mode, CVC provides the fastest design elaboration of any commercial Verilog simulator and offers an XL style interactive command debugger. CVC's interactive debugger has been extended to include gdb programming language debugging features. CVC also supports wave form debugging using either the P1364 VCD value change dump format or the SpringSoft (Debussy) Fsdb format.

Accurate Delay and Edge Exact Simulation

With CVC there is no need to accept the inconveniences, short cuts and lack of backward compatibility of other Verilog simulators. CVC does not sacrifice simulation accuracy or require cycle based assumptions or symbolic simplifications to achieve fast simulation. All edges and accurate delay Verilog constructs are preserved and rapidly simulated. During initial RTL encoding, fast elaboration eliminates the need to wait around for your design to finish elaborating. When compiled mode is selected, RTL designs simulate up to 65 times faster than in interpreted mode.

About Pragmatic C Software

Pragmatic C Software is a privately held Minneapolis based company that has been providing EDA solutions for the last 20 years. In addition to CVC, Pragmatic C has developed the Vcmp Valid Logic to Verilog net list translator, the first elaborator for the Chronologic VCS simulator, and the digital Verilog simulation engine for the Antrim Design Systems Verilog AMS simulator.

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